IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): An image display apparatus comprising:

a plurality of display pixels arranged in a matrix ~~in order~~ to ~~perform~~provide image display, each of said display ~~pixel~~pixels having a pixel electrode and a pixel switch connected to said pixel electrode in series;

a plurality of memory elements for storing display data;

~~an~~ image signal generating means for outputting a given image signal based on said display data;

B1 cont

a group of signal lines for connecting said image signal generating means to ~~said~~a group of pixel switches; and

~~a~~ display image selection means for writing said image signal in a given display pixel through said group of signal lines and ~~said~~a group of pixel switches,

wherein each basic unit of said memory element comprises a memory switch; a memory capacitor connected to said memory switch; an amplifier field-effect transistor (FET) of which a gate is connected to said memory capacitor; and ~~a~~ refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET.

Claim 2 (Original): An image display apparatus according to claim 1, wherein each of said plurality of display pixels is a liquid crystal display pixel having

a counter electrode and a liquid crystal region between said pixel electrode and said counter electrode.

Claim 3 (Original): An image display apparatus according to claim 2, wherein said plurality of display pixels have an optical reflecting plate.

Claim 4 (Original): An image display apparatus according to claim 1, wherein said plurality of display pixels, said group of signal lines and said image signal generating means are formed on a single transparent substrate.

Claim 5 (Original): An image display apparatus according to claim 1, wherein said pixel switch is a thin-film transistor (TFT).

Claim 6 (Original): An image display apparatus according to claim 5, wherein said pixel switch is a polycrystalline Si thin-film transistor (poly-Si TFT).

Claim 7 (Original): An image display apparatus according to claim 6, wherein said memory switch is a polycrystalline Si thin-film transistor (poly-Si TFT).

Claim 8 (Original): An image display apparatus according to claim 6, wherein said amplifier EFT is a polycrystalline Si thin-film transistor (poly-Si TFT).

Claim 9 (Original): An image display apparatus according to claim 1, wherein said memory capacitor is a capacitor between a gate and a channel of said amplifier FET.

Claim 10 (Original): An image display apparatus according to claim 6, wherein said memory capacitor is a capacitor between a gate and a channel of said polycrystalline Si thin-film transistor (poly-Si TFT).

Claim 11 (Currently Amended): An image display apparatus according to claim 1, wherein ~~the other end of~~ said memory capacitor is further connected to a wire to which a preset voltage is applied.

Claim 12 (Currently Amended): An image display apparatus according to claim 1, wherein ~~the other end of~~ said memory capacitor is further connected to an indium tin oxide (ITO) thin film to which a preset voltage is applied.

Claim 13 (Currently Amended): An image display apparatus according to claim 1, wherein ~~the other end of~~ said memory capacitor is further connected to a source of said amplifier FET.

Claim 14 (Currently Amended): An image display apparatus according to claim 1, wherein ~~the other end of~~ said memory capacitor is further connected to a drain of said amplifier FET.

Claim 15 (Currently Amended): An image display apparatus according to claim 1, wherein a drain of said amplifier FET is connected to ~~a~~ voltage applying means.

Claim 16 (Currently Amended): An image display apparatus according to claim 1, wherein a source of said amplifier FET is connected to ~~a~~ voltage applying means.

Claim 17 (Currently Amended): An image display apparatus according to claim 1, wherein a plurality of basic units of said memory elements are connected to one another by a data ~~lines~~line, and said amplifier FET is connected to said data line through a selection switch.

Claim 18 (Original): An image display apparatus according to claim 17, wherein said selection switch is a polycrystalline Si thin-film transistor (poly-Si TFT).

Claim 19 (Original): An image display apparatus according to claim 18, wherein said selection switch is a polycrystalline Si thin-film transistor (poly-Si TFT) which is diode-connected and made short circuit in the drain and the source.

Claim 20 (Original): An image display apparatus according to claim 17, wherein said selection switch is a p-n junction diode using a polycrystalline Si thin film.

Claim 21 (Original): An image display apparatus according to claim 17, wherein said basic units of the memory elements are arranged in a matrix along a group of data lines extending in a y-direction, and said memory switch and said selection switch in the individual basic unit are connected to the same data line.

Claim 22 (Original): An image display apparatus according to claim 17, wherein said basic units of the memory elements are arranged in a matrix along a group of data lines extending in a y-direction, and said memory switch and said selection switch in the individual basic unit are connected to the data lines different from each other.

Claim 23 (Original): An image display apparatus according to claim 17, wherein said basic units of the memory elements are arranged in a matrix along a group of data lines extending in a y-direction, and said data lines are arranged by n line units in a case where unit display data composed of n bits is stored by n basic units of said memory elements.

Claim 24 (Currently Amended): An image display apparatus according to claim 4, wherein a lighting means to the display pixels is provided on a surface of said transparent substrate opposite to the surface on which the display

pixels, the group of signal lines and the image signal generating means are arranged, and ~~a~~ black matrix shielding means is arranged between said transparent substrate corresponding to ~~the~~ back portions of said memory elements and said lighting means.

Claim 25 (Original): An image display apparatus according to claim 17, wherein a gate of complementary metal-oxide-semiconductor (CMOS) inverter is connected to said data line.

Claim 26 (Currently Amended): An image display apparatus according to claim 1, wherein said image signal generating means has ~~a D~~adigital-to-analog converting means for generating an image signal from display data stored in said memory element.

Claim 27 (Currently Amended): An image display apparatus according to claim 2, wherein said image signal generating means has ~~a D~~adigital-to-analog converting means for generating an image signal from display data stored in said memory element, and said ~~D~~adigital-to-analog converting means has a function of selectively outputting substantially two kinds of image signal voltages to the same display data.

Claim 28 (Currently Amended): An image display apparatus comprising:

a plurality of display pixels arranged in a matrix in order to ~~perform~~provide image display, ~~said~~each display pixel having a pixel electrode and a pixel switch connected to said pixel electrode in series;

~~an~~ image signal generating means for outputting ~~a given~~an image signal based on digital display data;

a group of signal lines for connecting said image signal generating means to ~~said~~a group of pixel switches; and

~~a~~ display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches, at least said plurality of display pixels, said group of signal lines and said image signal generating means being formed on a single transparent substrate,

wherein said image signal generating means has a reference voltage generating circuit using a boron-doped polycrystalline Si (poly-Si) thin-film resistor.

Claim 29 (Currently Amended): A method of driving an image display apparatus, said image display apparatus comprising:

a plurality of display pixels arranged in a matrix in order to ~~perform~~provide image display, ~~said~~each display pixel having a pixel electrode and a pixel switch connected to said pixel electrode in series;

~~an~~ image signal generating means for outputting ~~a given~~an image signal based on display data, said image signal generating means having a plurality of memory elements for storing said display data;

a group of signal lines for connecting said image signal generating means to ~~said~~a group of pixel switches; and

~~a~~ display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches,

wherein each basic unit of said memory element comprises a memory switch; a memory capacitor connected to said memory switch; and ~~a~~ refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor, and

~~operation of~~wherein reading of the display data from said memory element is included in ~~the~~a refreshing operation to said memory element using said refreshing operation means.

Claim 30 (Currently Amended): A method of driving an image display apparatus according to claim 29, wherein the ~~operation of~~ reading operation of the display data from said memory element is substantially equal to the refreshing operation to said memory element using said refreshing operation means.

Claim 31 (Currently Amended): A method of driving an image display apparatus, said image display apparatus comprising:

a plurality of display pixels arranged in a matrix in order to ~~perform~~provide image display, ~~said~~each display pixel having a pixel electrode and a pixel switch connected to said pixel electrode in series;

~~an~~ image signal generating means for outputting ~~a given~~an image signal based on display data, said image signal generating means having a plurality of memory elements for storing said display data;

a group of signal lines for connecting said image signal generating means to ~~said~~a group of pixel switches; and

~~a~~ display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches,

wherein each basic unit of said memory element comprises a memory switch; a memory capacitor connected to said memory switch; and ~~a~~ refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor, and

wherein writing of the display data to said memory element is performed based on address data, and refreshing to said memory element using said refreshing operation means is performed by sequentially scanning.

Claim 32 (Currently Amended): A method of driving an image display apparatus, said image display apparatus comprising:

a plurality of display pixels arranged in a matrix in order to ~~perform~~provide image display, ~~said~~each display pixel having a pixel electrode and a pixel switch connected to said pixel electrode in series;

~~an~~ image signal generating means for outputting ~~a given~~an image signal based on display data, said image signal generating means having a plurality of memory elements for storing said display data;

a group of signal lines for connecting said image signal generating means to ~~said~~a group of pixel switches; and

~~a~~ display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches,

wherein each basic unit of said memory element comprises a memory switch; a memory capacitor connected to said memory switch; and ~~a~~ refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor, ~~and~~

wherein a plural number of said memory elements are connected to a common data line, and

wherein the refreshing to said memory element using said refreshing operation means is performed by initially outputting the display data to said data line; ~~and~~ further amplifying a voltage level of said display data written in said data line; and then rewriting the amplified voltage of said display data from said data line.

Claim 33 (Currently Amended): A method of driving an image display apparatus, said image display apparatus comprising:

a plurality of display pixels arranged in a matrix in order to ~~perform~~provide image display, ~~said~~each display pixel having a pixel electrode and a pixel switch connected to said pixel electrode in series;

~~an~~ image signal generating means for outputting ~~a given~~an image signal based on display data, said image signal generating means having a plurality of memory elements for storing said display data;

a group of signal lines for connecting said image signal generating means to ~~said~~a group of pixel switches; and

~~a~~ display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches,

wherein each basic unit of said memory element comprises a memory switch;

a memory capacitor connected to said memory switch; and ~~a~~ refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor, ~~and~~

wherein a plural number of said memory elements are connected to a common data line, and

wherein the refreshing to said memory element using said refreshing operation means is performed by initially outputting the display data to said data line; and directly rewriting the voltage of said display data from said data line.

Claim 34 (Currently Amended): A method of driving an image display apparatus according to ~~any one of~~ claim 32 ~~and~~or claim 33, wherein the writing of the display data to said memory element is performed by address data~~rewriting part of said display data output from said memory element to said data line, and then rewriting said display data from said data line~~.

Claim 35 (Currently Amended): A method of driving an image display apparatus, said image display apparatus comprising:

a plurality of display pixels arranged in a matrix in order to ~~perform~~provide image display, ~~said~~each display pixel having a pixel electrode and a pixel switch connected to said pixel electrode in series;

~~an~~ image signal generating means for outputting ~~a given~~an image signal based on display data, said image signal generating means having a plurality of memory elements for storing said display data;

a group of signal lines for connecting said image signal generating means to ~~said~~a group of pixel switches; and

~~a~~ display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches,

wherein each basic unit of said memory element comprises a memory switch; a memory capacitor connected to said memory switch; and ~~a~~ refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor, and

wherein a driving pulse for driving said display image selection means and a driving pulse for driving said refreshing operation means are the same driving pulse branched from a single input.

Claim 36 (Currently Amended): A method of driving an image display apparatus, said image display apparatus comprising:

a plurality of display pixels arranged in a matrix in order to ~~perform~~provide image display, ~~said~~each display pixel having a pixel electrode and a pixel switch connected to said pixel electrode in series;

~~an~~ image signal generating means for outputting ~~a given~~an image signal based on display data, said image signal generating means having a plurality of memory elements for storing said display data;

a group of signal lines for connecting said image signal generating means to ~~said~~a group of pixel switches; and

~~a~~ display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches,

wherein each basic unit of said memory element comprises a memory switch; a memory capacitor connected to said memory switch; an amplifier field-effect transistor (FET) of which a gate is connected to said memory capacitor; and ~~a~~ refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET, and

wherein a read-out pulse is applied to a drain of said amplifier FET, when the display data is read out of said memory element.

Claim 37 (Currently Amended): A method of driving an image display apparatus, said image display apparatus comprising:

a plurality of display pixels arranged in a matrix in order to ~~perform~~provide image display, ~~said~~each display pixel having a pixel electrode and a pixel switch connected to said pixel electrode in series;

~~an~~ image signal generating means for outputting ~~a given~~an image signal based on display data, said image signal generating means having a plurality of memory elements for storing said display data;

a group of signal lines for connecting said image signal generating means to ~~said~~a group of pixel switches; and

~~a~~ display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches,

wherein each basic unit of said memory element comprises a memory switch; a memory capacitor connected to said memory switch; an amplifier field-effect transistor (FET) of which a gate is connected to said memory capacitor; and ~~a~~

refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET, and

wherein a read-out pulse is applied to a source of said amplifier FET_1 when the display data is read out of said memory element.

B' cancel.

Claim 38 (Currently Amended): A method of driving an image display apparatus according to ~~any one of~~ claim 35 ~~and~~or claim 37, wherein an amplitude of voltage driving said memory switch is larger than an amplitude of read-out pulse voltage applied to the drain or the source of said amplifier FET.